TEMPORAL AND SPATIAL MODELING OF ANALOG MEMRISTORS

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TEMPORAL AND SPATIAL MODELING OF ANALOG MEMRISTORS

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To my parents and sister

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SUMMARY

As silicon meets its performance limits, new materials and methods for advancing computing and electronics as a whole are being intensely researched, as described in Chapter 1. Memristors are a fusion of these two research areas, with new materials being pursued concurrently to development of novel architectures to take advantage of these new devices. A background of memristors and an overview of different memristive developments in the field are reviewed in Chapter 2.

Chapter 3 delves into the physical mechanisms of analog memristors. To investigate and understand the operation of analog memristors, a finite element method model has been developed.

More specifically, the devices simulated include a simple memristor simulation where the lithium ions (dopants) are confined to the device, but allowed to move in response to a voltage applied across the device. To model a more physical memristor, charge carrier mobility dependence on dopant levels was added to the device, resulting in a simulated device that operates similarly to the first simulation. Thereafter, the effect of varying geometries was modeled, and it was determined that both the speed and the resistance change of the device were improved by increasing the ratio of the top and bottom metal contact lengths in a restrictive flow geometry. Finally, the effect of dopant removal was investigated. It was determined that if the greatest change in resistance is required, then the removal of dopants is the optimal operating regime for an analog memristor.

Through a greater understanding of analog memristors developed by the simulation described herein, researchers will be able to better harness their power and implement them in bio-inspired systems and architectures.

CHAPTER I

INTRODUCTION

1.1 Motivation

Since the invention of the transistor by Bardeen, Brattain, and Shockley [2] computation has been dominated by silicon-based transistors. Despite the strong performance record of Moore's Law for more than six decades, researchers can now see the functional limits for silicon-based transistors [44]. As shown in Figure 1, it is theorized that as the distance between the source/drain contacts and the gate of the transistor continue to shrink in order to fit more transistors in a limited space, parasitics will eventually dominate device performance. Presently, chip manufacturers are at the 22 nm node, edging on the territory where parasitics will begin to dominate transistor performance [44].

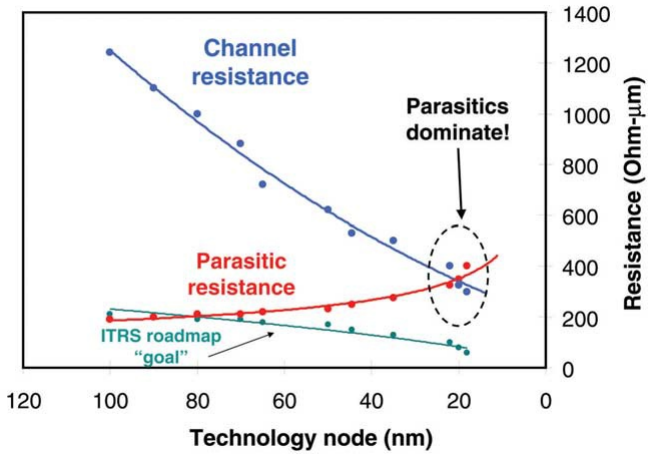

Figure 1: Estimated planar CMOS parasitic (red) and channel (blue) resistance vs. technology node. If present trends continue, parasitic resistance will dominate device performance [44]

1.2 Background

What can be done to alleviate this quickly-approaching halt in computational advances? There are two different approaches that are presently being researched. The first solution, and probably the more conservative of the two approaches, is to replace the channel material with a material that has higher hole and electron mobility than that of silicon. The second proposed solution is to transition over to an entirely new computational architecture.

The first solution to improve the performance of transistors by replacing the channel material with one that has a higher hole and electron mobility than that of silicon is relatively conservative because a complete overhaul of the computing architecture is largely unnecessary. Computation would still be performed in the same way as it is presently, but the devices used in computation would be improved. Materials proposed to improve the charge carrier mobilities of the channel include SiGe [13], GaAs [27], carbon nanotubes [24], and graphene [5] among others.

A second solution to the eventual halt in computational advances using present-day silicon-based systems is to revamp the entire computing architecture. What architecture would be an improvement to the silicon status-quo? Mead contends that an architecture based on performing computations similarly to the human brain, termed neuromorphic computing could improve computation on many levels [14]. Some of the key improvements would come in terms of power consumption, parallelization, and being able to solve poorly-conditioned problems.

The power advantages of neuromorphic computing are obvious in the case of cochlear implants. The inner ear has the capability to run on just 14 micro-watts[32]. This means that the inner ear could run on a typical AA battery for 15 years. Using a traditional Digital Signal Processor, cochlear implants can be implemented using 5mW. By implementing the cochlear implant in silicon using sub-threshold transistors and neuromorphic computing paradigms, the same implant is implementable using

just .25mW[32]. However, we are still far from matching the 14 micro-watts used in nature to run the inner ear. Clearly, there is still room for improvement over present-day neuromorphic implementations, but the neuromorphic architecture implemented in silicon is a step in the right direction.

In addition to power savings, computing similarly to the human brain has the advantage over present digital computing devices of being massively parallel. This massively parallel architecture results in an extremely robust system. The loss of a small percentage of neurons in the human brain results in no discernible loss in performance. However, the loss of even a single transistor in today's silicon-based computing systems can result in a loss of complete computing capability.

Lastly, the human brain can use ill-defined inputs and produce approximate outputs. This point is clear in the area of speech recognition. Many lines of code go into extremely elaborate algorithms to create digital speech recognition software that doesn't even work all that well even after it has been calibrated for a specific user. However, the human brain doesn't run into this problem at all. Business transactions occur all over the world between two people with a common language without the need of a calibration between the two. This is because the human brain is able to accept an approximate input (a non-native English speaker with a pronounced accent) and produce an understanding of the communication by a native English speaker.

1.3 Organization of thesis

This thesis explores the modeling of analog memristors for neuromorphic computing applications. The computational simulations will advance the understanding of analog memristors. The subsequent chapters will cover the physics behind memristor operation and the different memristor implementations as well as a Finite Element Method approach to modeling memristors. Chapter two of this thesis will cover the

theory, history, and development of memristors beginning with the original theorization of the necessity of a memristor device [10] and ending with the most recent analog memristor devices. Chapter three of this thesis will then cover background of the numerically simulated two-dimensional memristors and then will explain the physics used in the memristor model. After explaining the physics, the results of the memristor simulation will be divulged. Finally, chapter four of this thesis will disseminate the conclusions to be drawn from this research and future directions for this research.

CHAPTER II

MEMRISTORS AND MEMRISTIVE DEVICES

2.1 Background

Originally theorized by Chua in 1971 [10], the memristor is the "missing" 4th circuit element that relates the fundamental physical electromagnetic quantification parameter of magnetic flux, ϕ, to the fundamental physical electromagnetic quantification parameter of electric charge, q. In practice, one cannot measure either fundamental parameter, ϕ or q, but can instead measure current, i, and voltage, v. Moreover, Maxwell's equations dictate that there is no direct fundamental linkage between the fundamental physical electromagnetic quantification parameter of magnetic flux, ϕ, and the fundamental physical electromagnetic quantification parameter of electric charge, q. Instead, Maxwell describes an interplay between the time derivatives of these fundamental parameters. The three traditional linear circuit elements, resistors, capacitors, and inductors relate measurable quantities, current and voltage, to either themselves (resistor with resistance R relates measurable current, i, to measurable voltage v by v=Ri and dv=Rdi) or relate the measurable quantities to the fundamental physical parameters, ϕ or q. Specifically for the latter, an Inductor with inductance L, relates measurable current, i to the fundamental magnetic flux, ϕ, by dϕ=Ldi while a capacitor with capacitance C relates measurable voltage, v, to the fundamental unit of charge, q, by dq=Cdv. The Chua-suggested role of a memristor, with memristance M is to relate fundamental charge, q, to fundamental magnetic flux, ϕ, by dϕ=Mdq. This sets the memristor apart as a circuit element that differs from all others in that it does not involve either measurable current or voltage. Thus, the fundamental behavior of a memristor, dϕ=Mdq, cannot be directly measured but

instead is functionally inferred by observations of its current and voltage. This functional behavior can be implemented with a variety of devices including those proposed by Tellgen who suggested the existence of a "gyrator" and implemented in modern magneto-electric composite devices [49] or alternatively as a memristor as described by HP Labs [40]. It should also be noted that linear electronic theory dictates that resistors dissipate real power since resistors involve only measurable quantities. Contrarily, both inductors and capacitors dissipate only reactive power, essentially only storing energy with ideally zero loss. A key feature of a memristor can be defined as the ability to store and later recover both voltage and charge as defined by the relationship dϕ=Mdq. In the magneto-electric composites, charge storage is obtained via the piezoelectric material while magnetic flux storage is realized by the magnetostrictive materials. The energy is recovered when the electric/magnetic field induced strain is subsequently relaxed. In the memristors, voltage and charge are stored and recovered via mechanisms of dopant drift and subsequent diffusion. This mechanism will be detailed in a later section. For completeness, as stated above, no fundamental relationship (scalar or vectored) is presently known connecting magnetic flux to electronic charge. Conversely, Maxwell's equations suggest a vectored relationship between the time derivatives of magnetic flux and the time derivatives of electric field. Thus, by transduction, a relationship is formed between the time derivatives of charge and time derivatives of magnetic flux.

Chua asserted that this "missing" fundamental relationship between electric charge and magnetic flux is not necessary for the missing circuit element to be implemented [10]. Specifically, if the time derivatives of magnetic flux and time derivatives of electric charge are related to the electromotive force (potential) and current, memristance can be defined in terms of only the measurable quantities, current and voltage as shown in equations 1-3. A key point relevant for linear circuit theory as originally proposed by Chua in equation 3 describes a continuous relationship between voltage

and current. Indeed, Chua clearly showed in figure 4 of his seminal theorization[10] that his original description was an analog circuit element.

$$M(q) = \frac{d\phi_M}{dq} \tag{1}$$

$$M(q) = \frac{\frac{d\phi_M}{dt}}{\frac{dq}{dt}} = \frac{V}{I} \tag{2}$$

$$V(t) = M(q(t)) \cdot I(t) \tag{3}$$

The overwhelming majority of presently demonstrated memristors or resistance switching devices show abrupt current/voltage characteristics and do not reflect the continuously changing resistance response of an analog memristor. Thus, the term memristor has been generally expanded to include digital memristance, i.e. any resistance change that has a memory effect dependent on the previous current through the device. Given this accepted widening of the term memristance beyond Leon Chua's original description, in this paper, all two terminal devices that undergo a resistance change dependent on the previous charge flow are termed a memristor. For clarity, if a memristor has one or more sudden abrupt resistance changes, we define it herein as a digital memristor. If there is no sudden state change but a gradual continuous resistance change, we define this as an analog memristor.

Both digital and analog memristors find applications in the field of computation. Digital memristors have been shown to implement logic gates [22] and reprogrammable circuitry [38] while analog memristors are well-suited for neuromorphic computing applications [19]. Neuromorphic computing is a biologically-inspired architecture that seeks to compute similarly to the brain with an interconnect of low-power synapses and neurons. The neuromorphic computing architecture is a proposed solution to replace present-day computing devices which will begin to approach performance limits due to excess heat and power consumption. The memristor is a key

enabling device for neuromorphic computing since it exhibits a conductance response similar to that of a synapse.

Because neuromorphic computing seeks to compute using a minimal amount of power, memristors used to emulate synapses need to be conductive devices. Additionally, if the neuromorphic implementation is to be truly biologically inspired, the memristors used in the neuromorphic implementation need to exhibit analog behavior. Based on these two constraints, the devices that exhibit an insulator to metallic transition are unsuitable for neuromorphic computing since the insulating phase yields a device with extremely high resistance and thus relatively high power requirements. It is for the same reasons that we believe that a semiconductor device that undergoes a controlled dopant change to be best suited for neuromorphic computing applications. Such a device is modeled in this research.

2.2 Significant Memristive Devices

2.2.1 The digital memristor switch

The first memristor implementation claimed was the HP Labs digital resistive switch which consists of a TiO_{2-x} film sandwiched between two Pt electrodes [40] but since then and before this claim, many devices/materials have exhibited digital memristive behavior [42, 33, 31, 28, 23, 21, 18, 9, 8, 4]. The HP device is representative of most of the digital memristors in the literature and has two stable states which will be referred to as the conductive and insulating states. The present state of the device is determined by the previous inputs to the device in a limited sense but unlike the proposal of Chua, is not dependent on the entire integrated current history of the device. It is necessary to qualify the previous statement with a brief physical explanation of the digital memristor. The change in resistance in the device is facilitated by the formation of conductive filaments made of TiO_{2-n} magnéli phases where n=4 or 5 that form due to oxygen dopant drift [20]. During the electro-forming cycle wherein

the small filaments are created via a current limited breakdown, a dramatic increase in temperature in resistive oxide switches occurs which greatly enhances dopant drift [15]. This oxygen drift can even lead to damage to the memristor contacts[48]. Evidence for the creation of filamentary conduction paths has been confirmed using high-resolution transition electron microscopy [20], concurrent spatially-resolved x-ray absorption and electron diffraction [36], and conductive atomic force microscopy [7] among other methods.

The relevance of the physical operation of these digital memristors to the suggestion that these digital devices do not constitute a complete implementation of the original Chua-proposed memristor is based on the assertion that only a partial history of the current voltage characteristic effects the resistance. Consider the case when the digital memristor is in its high-resistance, insulating, state. If a bias is applied that drifts oxygen dopants to form a conductive filament, the resistance changes quickly to the conductive state. Next, if a bias is applied with the same polarity as the previous case, the resistance does not change significantly, since a filament has already formed and thus the resistance of the memristor would remain in the conductive state. In this second application of a bias, the resistance state has not changed. Therefore, the present state of a digital memristor is a function of a limited history of inputs to the device. Additional material systems have exhibited the same resistive switching behavior used to describe the digital memristor including ZrO_2 [23], $Pr_{.7}Ca_{.3}MnO_3$ [28], NiO [31], Nb_2O_5 [33], CeO_x [42], $SrTiO_x$ [8], Al_2O_3 [18], Ta_2O_5 [9], $SrZrO_3$ [4]. Because of the digital nature of the resistive switch memristors, they are well-suited to digital logic, digital memory[39], and reconfigurable circuit applications[38].

2.2.2 Ag/Si graded memristor

An analog memristor based on a similar mechanism to the resistive switch has been developed [19]. This analog memristor uses Ag particles co-sputtered with Si in a

graded pattern and, just like in the resistive switching devices, the metal/insulator transition is controlled with an applied bias. However, unlike in the resistive switching memristor, a gradual resistance change is facilitated by the graded Ag doping, and a conduction front is formed instead of single conducting filaments. The Ag/Si analog memristor has demonstrated the ability to replicate basic synaptic functionality, suggesting that it as well as all of the analog memristors mentioned below, can be used in neuromorphic computing applications[19].

2.2.3 Spintronic memristor

A solid state spintronic memristor based on a semiconductor - ferromagnetic junction has been proposed [30]. The junction allows electrons of one polarity of spin to enter the ferromagnetic layer while the opposite spin electrons are blocked. This blockage produces a cloud of electrons with the spin polarity that is blocked. As voltage is increased in the device, the current through the junction saturates as the electrons with a polarity that allows them to pass through the junction are blocked by the cloud of electrons with the blocking spin. Thus, the conductivity of the device is a function of the current that has previously passed through the device.

2.2.4 Analog memristor based on mobile dopants

Another linear analog memristor based on dopant drift and diffusion instead of a semiconductor-ferroelectric junction was theorized in 1974 as an electrolytic cell with electrodes that effect the concentration of the electrolyte[29]. The cell appears as a resistor whose resistance is a function of the net current through the device. Additionally, as demonstrated by the memristor simulations described herein, a gradient in concentration of the ionic species in the electrolyte will change the doping profile and produce a change in resistance without the removal of ionic species. A solid-state implementation of this device has been developed [17]. In this implementation, lithium ions drift due to an applied bias which results in a change in doping profile

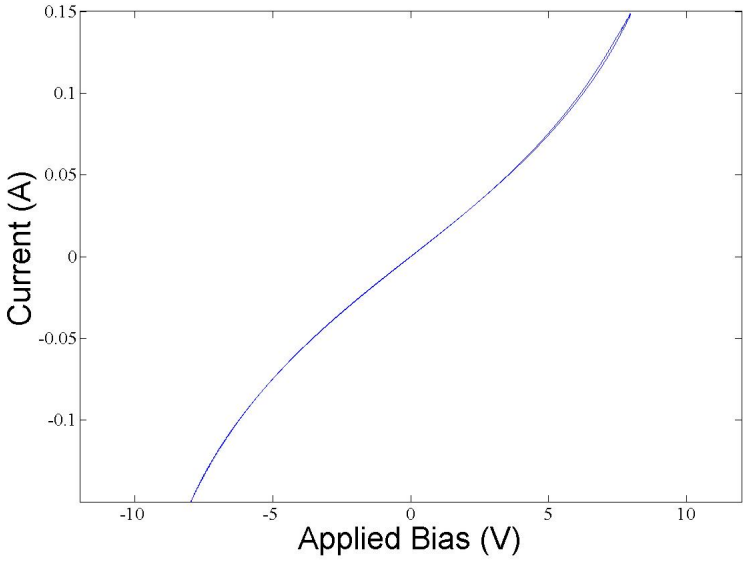

Figure 2: IV curve of $LiNbO_2$ memristor.

and thus a change in resistance. Lithium motion has been confirmed in $LiNbO_2$ using nuclear magnetic resonance[25]. Analog functionality is shown in the I-V curve in Figure 2 which has a striking similarity to Figure 4 from Chuas original active device implementation of the memristor [10].

Because of the large geometry, the lack of a set or reset voltage, and the independence of the memristance on scaling, it is theorized that the change in resistance observed in the lithium niobite memristor is due to the drift and diffusion of lithium which results in a (lithium) doping gradient and not a result of filamentary conduction. Nickel contacts are used in this device because Ni does not readily alloy with lithium [46]. However, lithium has been known to plate on metal contacts in solid-state batteries [3] which could result in the removal of lithium and the creation of acceptors.

2.2.5 WO_3 Memistor

The first analog memristor-like device developed was termed a "memistor" and was not connected to Chua's original theorization of the memristor because the device

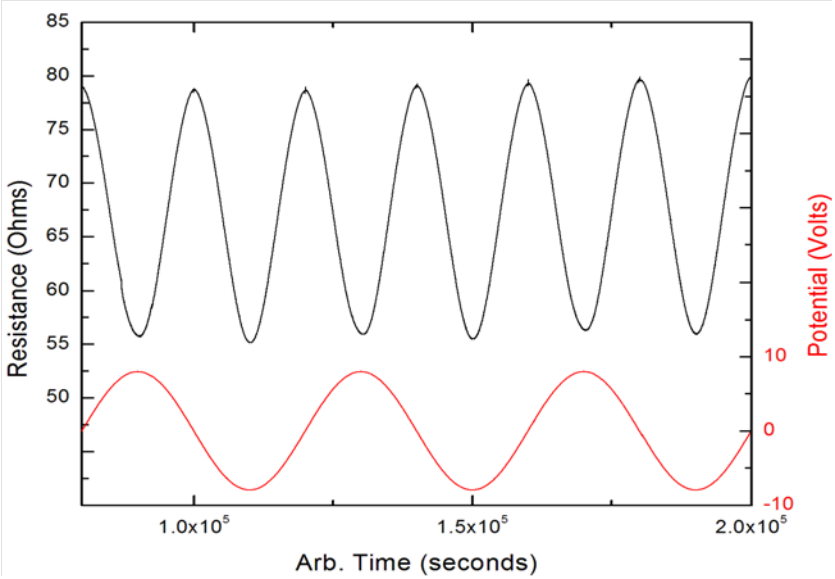

Figure 3: Sinusoidal voltage input (red) and resistance response of $LiNbO_2$ memristor (black).

had three terminals and it is unknown whether the authors tried to connect two of the terminals together as done in [6], but it is still worth noting this device since it is the first implementation of an analog device with a conductivity that depends on previous current inputs to the device. The memistor has a base WO_3 layer that is covered with a sandwich of SiO_2-Cr_2O_3-SiO_2. H^+ ions are injected from the Cr_2O_3 layer to dope the WO_3 film resulting in an increase in conductivity. The memistor has a resistance state that spans orders of magnitude (10^5 to 10^9 Ω). Despite having promising analog functionality, the tungsten oxide-based memistor suffered from reliability issues because the constant cycling of H^+ ions produced gas pockets under the contacts, much like the oxide resistive switch, which would lead to failure. It was theorized that reliability could be increased by doping the WO_3 film with metal ions instead of H^+ ions.

2.2.6 Organic Analog Memristor

An organic implementation of a three-terminal analog memristor has also been demonstrated [16]. The electrically active polyanaline layer is reversibly doped using either Li or Rb ions. In order to monitor both electronic and ionic currents, the device has three terminals, but two of the terminals are connected to ground, thus the device can ultimately be implemented with two terminals. The three terminal nature of the organic memristor was used to demonstrate the relationship between measured charge transfer with conductivity variation. A layer of polyaniline is used which is reversibly modulated between an insulating reduced state and a conductive oxidized state which has been confirmed in both time and space using space resolved Raman scattering [6].

Beginning with Chua's original formulation, memristor research has witnessed many innovative advances. The WO_3 memistor, although not connected to Chua's original idea, was one of the first devices to take advantage of dopant drift and diffusion to modulate the resistance of the device. Digital resistive switches exploit the same dopant drift and diffusion to create memristors that are well suited to digital logic and digital memory applications. Analog memristors, including the Si/Ag graded doped memristors, the lithium-containing memristor, and the organic memristor, are a quickly-emerging class of devices that are capable of emulating synapses in the brain and will be a critical enabling circuit element for neuromorphic computing architectures.

Table 1: Comparison of Memristive Devices

Material	Reference	Resistance Modulation Method
Original demonstration	[10]	Multiple Active Devices
TiO_2	[40]	Filament conduction
Ag/Si Graded Doping	[19]	Filament conduction front
Ferromagnetic-semiconductor junction	[30]	Spintronics
Electrolytic cell	[29]	Electrolyte species removal
Analog organic memristor	[16]	Cation drift and diffusion
Analog inorganic memristor	[17]	Cation drift and diffusion

CHAPTER III

SIMULATION OF MEMRISTIVE DEVICES

3.1 Methods

In order to gain a better understanding of the underlying physics of the analog memristors, a finite element simulation was developed to model analog memristor functionality. The simulated analog memristors operate by the gradual doping of a film using ions much like the memistor based on WO_3, the $LiNbO_2$ memristor, and the analog organic memristor. The finite element model is implemented as a 2D semiconductor in which mobile ions determine the doping profile in the device. While implemented as lithium ions in a p-type material in the present case, the physics represented herein describes any ion doped memristor or memistor. Simulations are divided into four cases. The geometry of the first case is a simple bar-type structure where dopants are restricted within the device. The second case introduces the dependence of hole mobility on the number of acceptors, a well-known phenomena in semiconducting materials. The third case explores different constrictive flow geometries and their effect on device performance,and the fourth case considers the effects of lithium extraction from the memristor.

The memristor finite element model was developed using the COMSOL Multiphysics platform. Because the relaxation times for holes and electrons are significantly shorter than that of lithium ions [43], the simulation was implemented using an iterative process where the solving of temporal lithium drift and diffusion was alternated with the solving of steady-state hole and electron movement with Poisson's equation. In order to insure stability in the transient solutions, meshing and time steps are chosen to satisfy the Courant condition [12]. Boundary conditions are chosen such

that electric field, hole current, and electron current have zero normal components except at the device contacts. In all simulations other than case 4, lithium ions are confined within the device. That is, the ionic current normal to the device at all edges is zero. In case 4, there is a fixed flux of lithium extracted at the bottom contact in the device, which models intercalation of mobile dopants into the device contact.

$$J_{Li} \cdot n = 0 \tag{4}$$

At the device metal contacts, infinite minority carrier recombination velocity is assumed. The applied voltage to the metal contact is equal to the Fermi level in the semiconducting memristor at the contact. Thus, the electrostatic potential at the contact is

$$\phi_E = V_{Bias} + \frac{kT}{q} ln \left(\frac{\frac{N_D - N_A}{2} + \sqrt{(\frac{N_D - N_A}{2})^2 + {n_i}^2}}{n_i} \right) \tag{5}$$

where ϕ_E is the electrostatic potential, V_{Bias} the applied bias, and N_A the concentration of acceptors, N_D the concentration of donors, and n_i the intrinsic carrier concentration.

Poisson's equation is solved to obtain the electrostatic potential in the simulated memristor due to holes, electrons and ions:

$$-\nabla \cdot (\epsilon \nabla \phi_E) \phi_E = q(p - n + N_D - N_A) \tag{6}$$

Where μ_{Li}, μ_p and μ_n represent the mobility of lithium, holes, and electrons respectively, D_{Li}, D_p, and D_n the diffusivities of lithium, holes, and electrons respectively, q the elementary charge, and ϵ the electric field. The mobilities and diffusivities are not constant in the simulated memristors. In the simulation of case 2, the mobility of holes is a function of the concentration of acceptors. In all cases, the diffusivity of lithium increases for increasing amounts of lithium [34]. An entropic term is introduced that inhibits lithium from reaching unphysical concentrations.

The continuity equations for lithium ions, holes and electrons are given by:

$$\frac{\partial Li_{vacancy}}{\partial t} = \frac{\partial N_A}{\partial t} = \frac{1}{q}\nabla \cdot J_{Li} \tag{7}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla \cdot J_p + \frac{\partial p}{\partial t} \mid_{Electron-HoleRecombination} \tag{8}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n + \frac{\partial n}{\partial t} \mid_{Electron-HoleRecombination} \tag{9}$$

Physical values have been used that describe a material with a layered structure, $LiCoO_x$, that reversibly intercalates and deintercalates lithium from $1 \geq x \geq .5$ that has a 2.7eV band gap when fully lithiated.

Models have been previously developed to describe memristor operation which include dopant drift due to an applied bias [37]. However, these simulations lack physical constraints on ionic concentrations , are implemented in one dimension, and neglect the effect dopant levels have on mobilities of charge carriers. The simulation described herein is implemented with more realistic physical details and in two dimensions, thus giving insight to the effect of geometry on device performance .

3.2 Results

3.2.1 Case 1: Simple bar geometry with closed boundaries

The memristor simulated in case 1 is defined by insulating boundaries for lithium in the entire device, constant hole mobility, and a bar-like geometry. Initially, the memristor simulated in case 1 has a homogeneous lithium concentration throughout the device (Figure 5). In these materials, lithium vacancies act as acceptors making the material predominantly p-type. However, as time increases, lithium is drifted away from the positively biased contact (located at 0 μm) towards the grounded contact (located at 2.0 μm). In the part of the device with increased lithium concentration, holes are filled while in the part of the device that lithium has decreased results in the

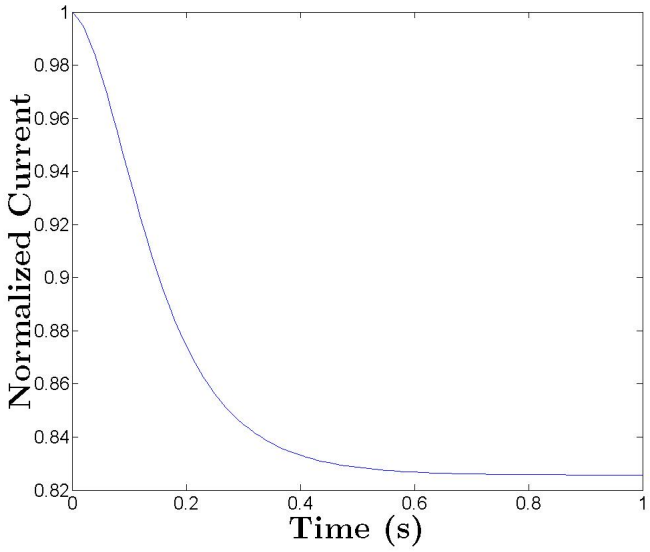

Figure 4: Case 1 current response to a constant bias of a simulated $LiNbO_2$ memristor.

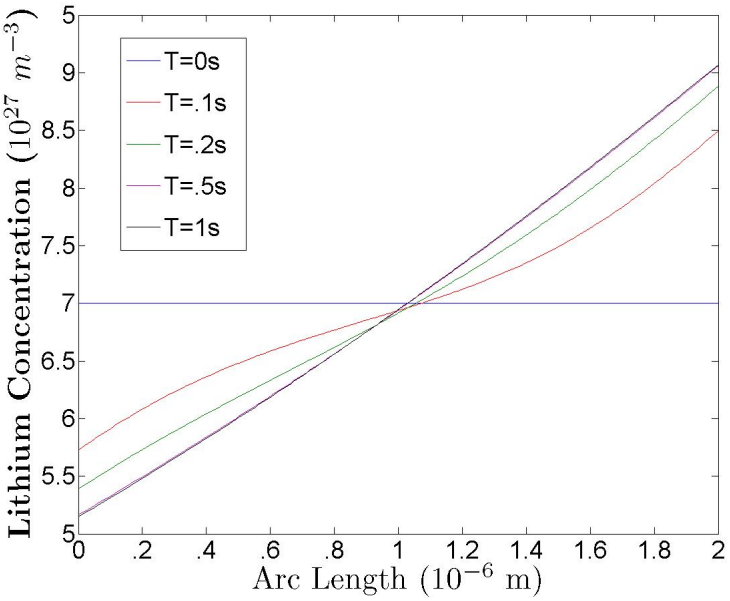

Figure 5: Case 1 temporal and spatial evolution of lithium concentration in an $LiNbO_2$ memristor.

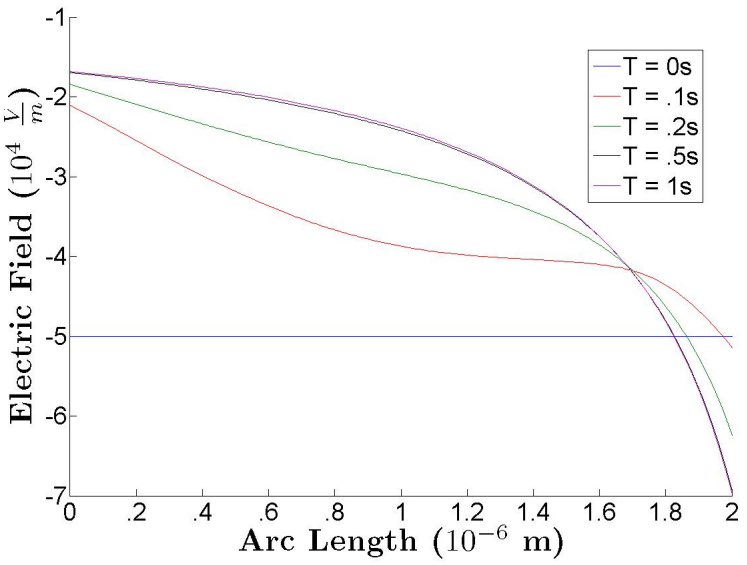

Figure 6: Case 1 temporal and spatial evolution of electric field in an $LiNbO_2$ memristor.

introduction of holes [1]. Thus the dopant levels in the device change as a function of time.

This evolution of lithium concentration in the device results in a simultaneously modulating electric field as shown in Figure 6. Initially, hole motion is completely drift mediated producing an electric field that is constant throughout the device. At T=.1s, the change in electric field is dominated by two factors. First, the areas where there is a gradient in holes (due to the change in lithium concentration) leads to a changing electric field. Additionally, as lithium approaches its stoichiometric concentration ($1{\cdot}10^{28}\frac{atoms}{m^3}$), a resistive area is formed leading to a more rapid increase in the electric field on the side of the device near the grounded contact. Later time steps are almost completely dominated by the latter effect as lithium vacancies and thus acceptors, plummet close to the grounded edge of the device. Eventually, the lithium concentration reaches a steady state as demonstrated by the leveling off of the device current (Figure 4). As the simulation reaches this steady-state, drift and diffusion balance which is facilitated by two separate phenomenon. First, there is an

entropic term which enforces volume constraints on the lithium. The entropic term is realized by an increase in the diffusion coefficient as the concentration of lithium increases and is adapted from a first-principles approach [34]. Because the part of the memristor with the lowest level of acceptors (highest concentration of lithium) has the greatest magnitude of electric field and thus the highest level of drift current, the magnification of the diffusivity in the same area leads to an equilibrium.

Additionally, as the lithium concentration is increased, the number of acceptors decreases thus causing the electrostatic potential to increase due to the logarithmic dependence of the electrostatic potential on dopants. Conversely, as the lithium concentration is decreased, the number of acceptors increases and thus the electrostatic potential decreases. Because lithium depletes in the area nearest to the positive bias, the electrostatic potential decreases while the grounded side of the device experiences an increase in the electrostatic potential. The raising of the electrostatic potential on the grounded side of the device and the lowering of the electrostatic potential on the positively-biased side of the device results in a decrease in the overall voltage drop across the device and thus a decrease in the drift component of current.

The steady state current change due to an applied bias in the case 1 device is 17.43% (Figure 4). This would correspond to an increase in resistance. Note that this current (resistance) change is only representative of a device with a homogeneous initial lithium concentration that is 70% of the stoichiometric concentration. Resistance changes will depend on device geometry and more strongly on the choice of initial doping, with larger doping changes supplied by doping selections closer to the stoichiometric value as demonstrated in case 4. The main contributions to the increase in resistance are the introduction of diffusion mediated hole movement and the formation of highly resistive areas with low concentrations of dopants that dominate the resistance profile of the device as is evident from the electric field profile.

3.2.2 Case 2: Dependence of charge mobility on dopant levels

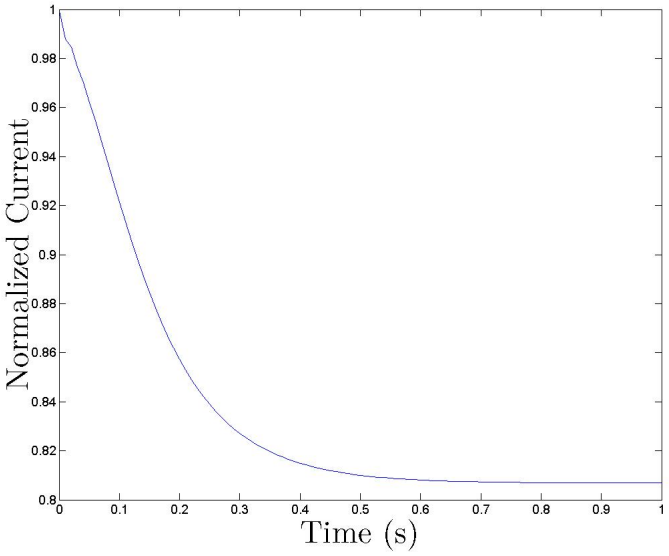

Figure 7: Case 2 current response to a constant bias of a simulated $LiNbO_2$ memristor.

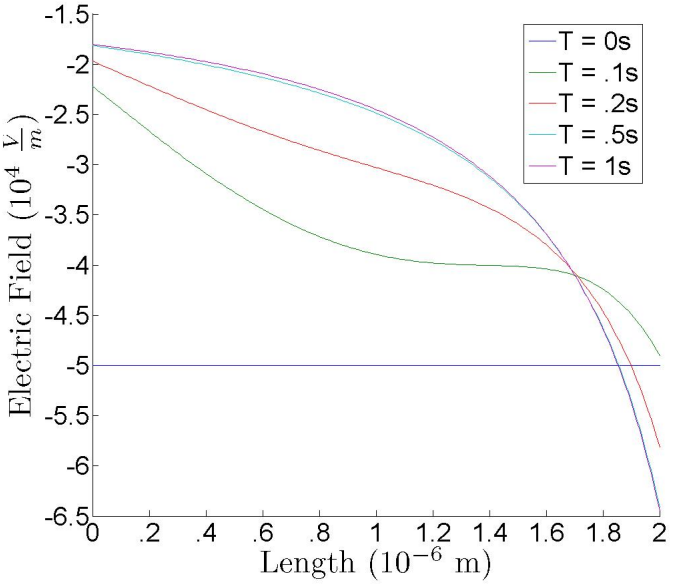

Figure 9: Case 2 temporal and spatial evolution of electric field in an $LiNbO_2$ memristor.

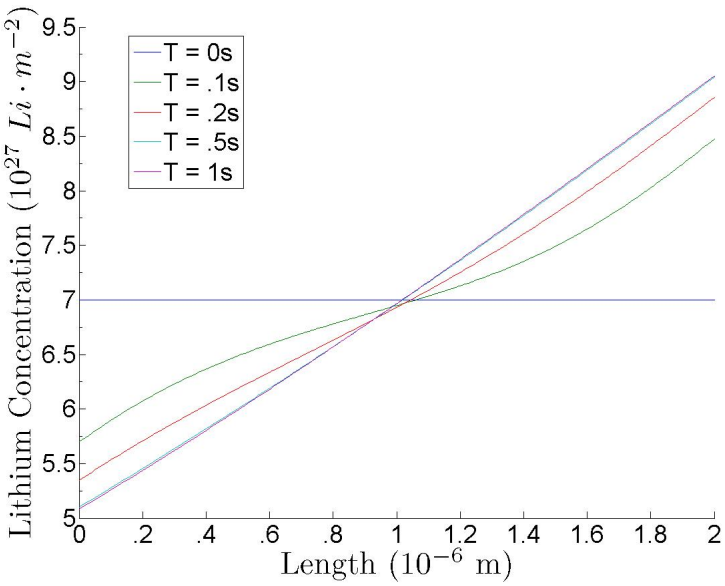

Figure 8: Case 2 temporal and spatial evolution of lithium concentration in an $LiNbO_2$ memristor.

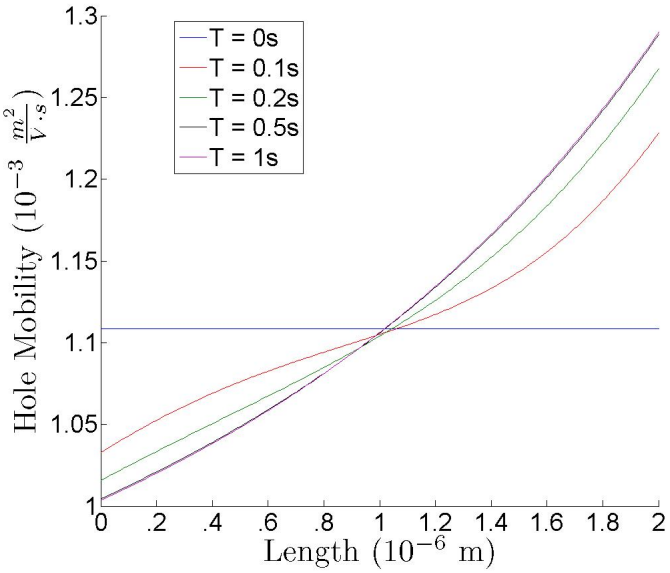

Figure 10: Case 2 temporal and spatial evolution of hole mobility in an $LiNbO_2$ memristor.

Case 2 differs from case 1 in that the mobility of holes in the device is dependent

on the concentration of acceptors. As the concentration of acceptors is increased, scattering also increases which is realized by a decrease in hole mobility:

$$\mu = \mu_{min} + \frac{\mu_o}{1 + \frac{N}{N_{ref}}^{\alpha}} \tag{10}$$

where μ_{min}, μ_o, and α are unknown for both $LiCoO_2$ and $LiNbO_2$, so the values μ_{min}=5 $\frac{cm^2}{V \cdot s}$, μ_o=9.20188 $\frac{cm^2}{V \cdot s}$, and α=.88 were used. As seen in Figures 8 and 9, the lithium and electric field evolutions do not differ dramatically from those in case 1. This similarity is not surprising since the mobility of the charge carriers in the device do not change significantly as shown in Figure 10. Nevertheless, there are slight differences most notably in the electric fields of case 1 and case 2. In case 1, the steady state (Time = 1s) electric field on the edge of the device where lithium is depleted is -16,800 $\frac{V}{m}$ and the electric field at the edge of the device where lithium has accumulated is -69,800 $\frac{V}{m}$. In case 2, the steady state (T = 1s) electric field on the edge of the device where lithium is depleted is -18,000 $\frac{V}{m}$ and the electric field at the edge of the device where lithium has accumulated is -64,400 $\frac{V}{m}$. Thus, the net effect of acceptor concentration dependent mobility is minimal, and results in the conductive area of the memristor in case 1 becoming less conductive while the resistive area becomes slightly less resistive. The net steady state current change from t=0s to t=1s is 19.3% in case 2 as shown in Figure 7, slightly increased from case 1.

3.2.3 Case 3: Varying constrictive flow geometry ratios

In addition to the hole mobility dependence on the number of acceptors as described in case 2, an additional variable that can affect both the speed and change in resistance is the geometry of the memristors. The third case modeled herein is the variation of memristor geometry. Three different geometries were investigated. Specifically, constrictive flow geometries with different ratios of the length of the top of the device with the length of the bottom of the device. Memristors with metal contact length

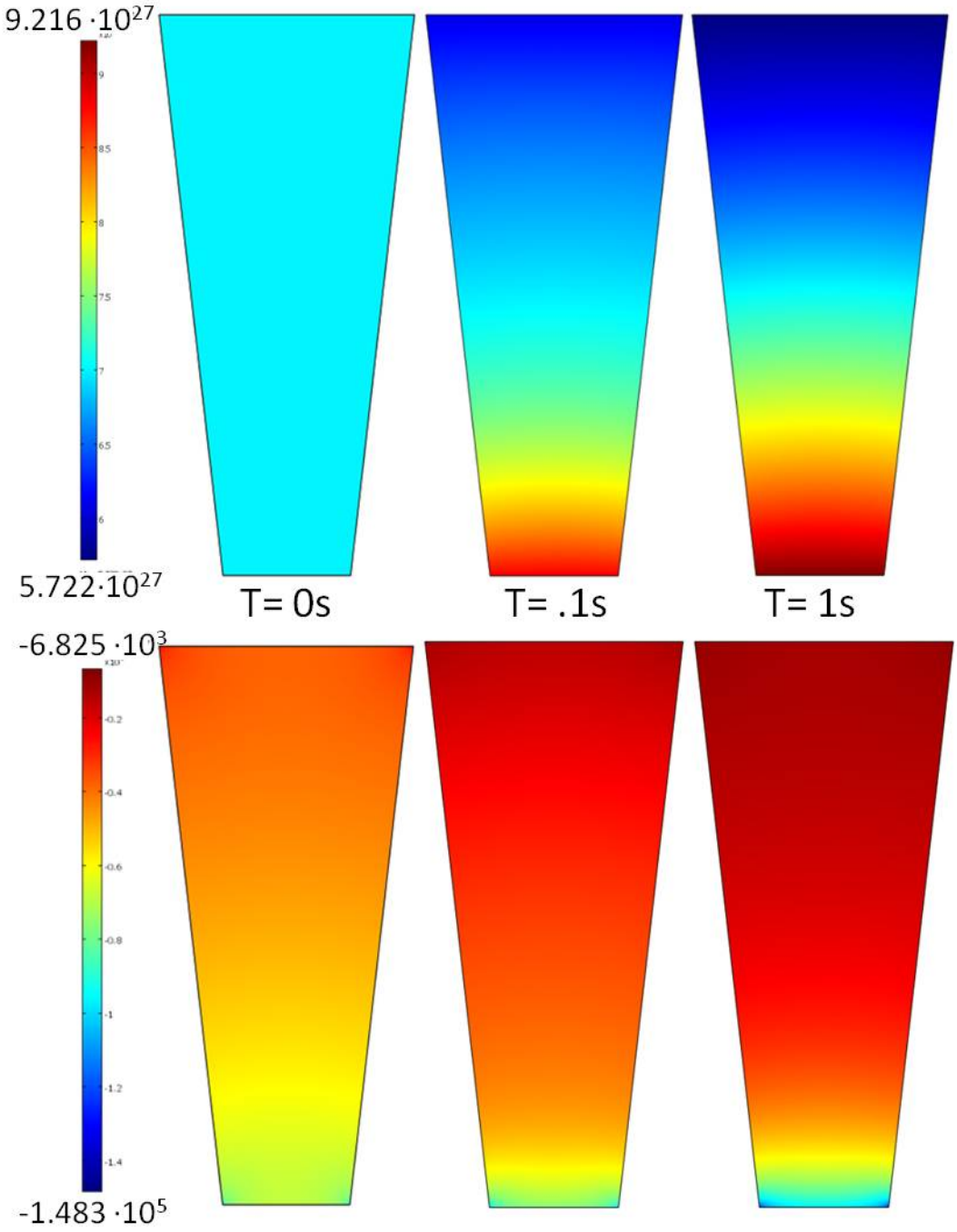

Figure 11: Lithium concentration(top) and electric field(bottom) evolution for the 2x constrictive flow geometry

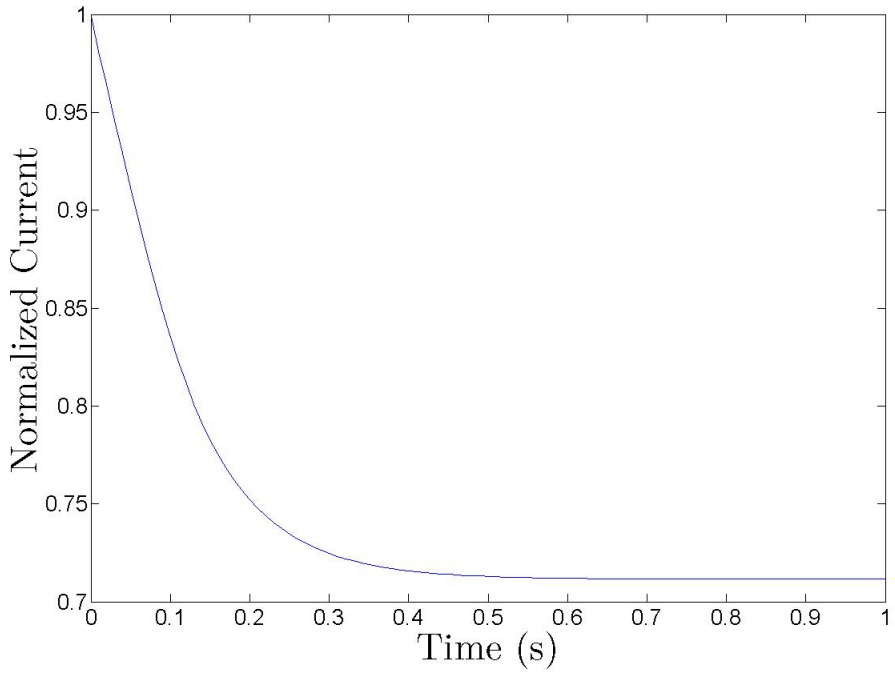

Figure 12: Temporal electronic current response for the 2x constrictive flow geometry

ratios of 2, 5, and 10 were simulated. In all three geometry configurations, a positive bias is applied to the top of the device where the length of the contact is greater and the bottom of the device is grounded. Thus, the movement of lithium is in the direction of the smaller contact and becomes constricted as shown by the geometries in Figures 11, 13, and 15 . The overall effect of the constrictive flow geometry is to facilitate areas of higher lithium concentration. This increased lithium concentration creates areas with higher resistance compared to those in case 1 which result in a bigger change in steady-state device current. The device with the top electrode being twice the size of the bottom electrode (the 2x geometry) has a homogeneous initial lithium concentration with an inhomogeneous resultant electric field due to current crowding at the bottom electrode as shown in Figure 11. As time progresses in the simulation, lithium is drifted to the bottom of the device, resulting in a highly resistive region. This highly resistive region in the 2x constrictive flow geometry

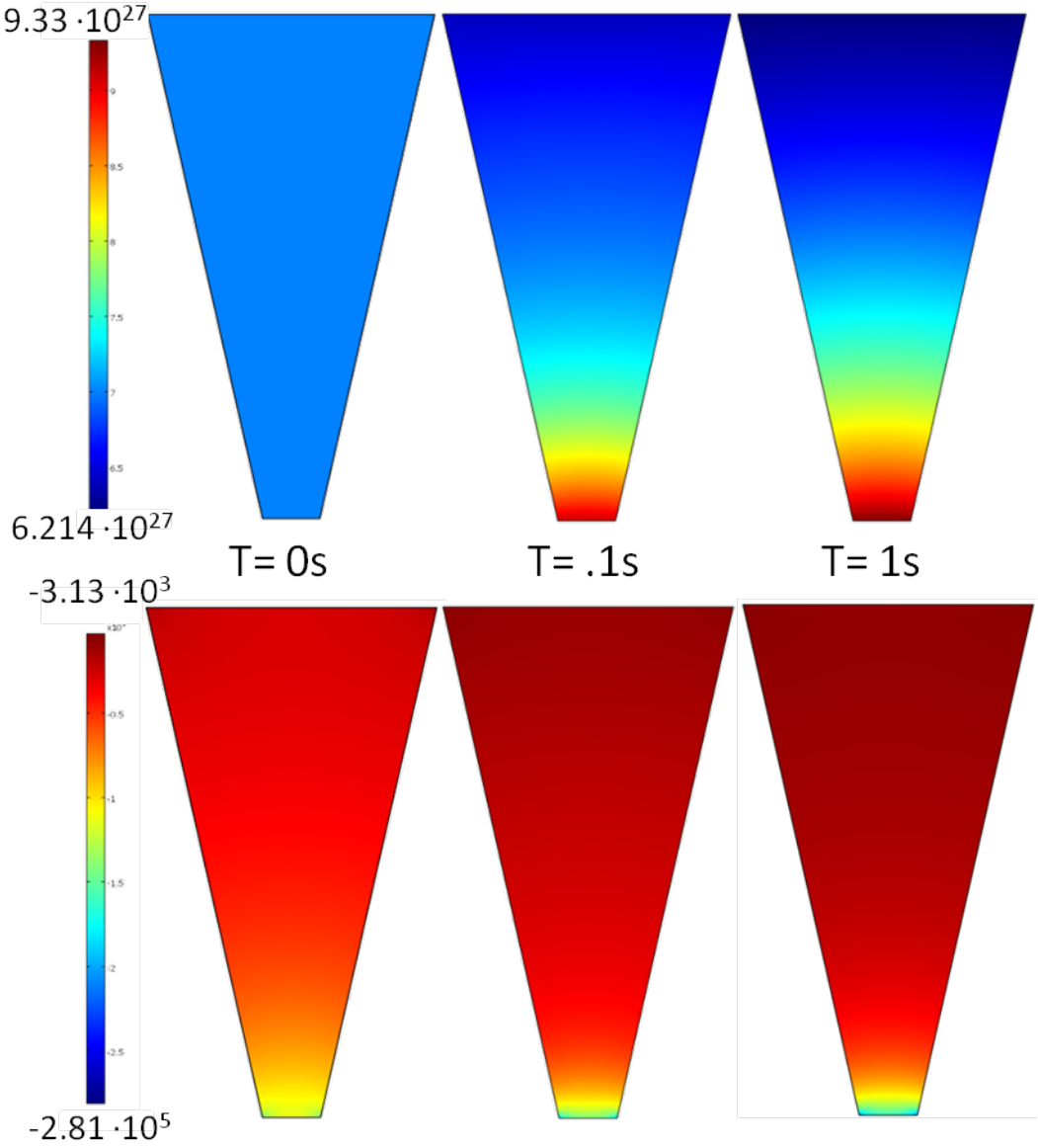

Figure 13: Lithium concentration(top) and electric field(bottom) evolution for the 5x constrictive flow geometry

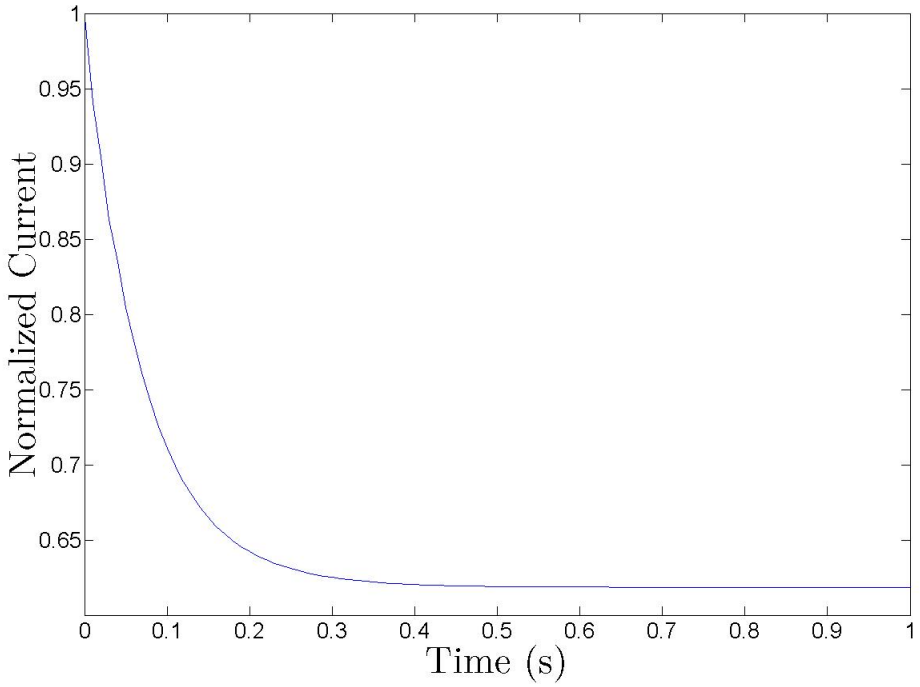

Figure 14: Temporal electronic current response for the 5x constrictive flow geometry

has a maximum lithium concentration of $9.22{\cdot}10^{27}\frac{atoms}{m^3}$ vs. $9.07{\cdot}10^{27}\frac{atoms}{m^3}$ for the constant geometry of case 1. The increase in maximum lithium concentration creates a greater gradient in acceptors and thus an increase in diffusion current. This increase in maximum lithium concentration for the 2x constrictive flow results in a change in current as shown in Figure 12 of 28.85%, more than 65% greater than that of case 1. The maximum lithium concentration increased to $9.33 \cdot 10^{27}$ in the 5x case. This increase in maximum lithium concentration results in a current change of 38.15% (Figure 14). The last constrictive flow geometry case simulated is a device that has a 10x ratio of the length of the top of the device to the length of the bottom of the device as shown in Figure 15. The maximum lithium concentration has once again increased and is $9.378{\cdot}10^{27}\frac{atoms}{m^3}$. This corresponds to a change in current of 42.18% as seen in Figure 16. The difference between the 5x to 10x case in terms of overall current change is much lower than the case 1 to 2x case current change. This current

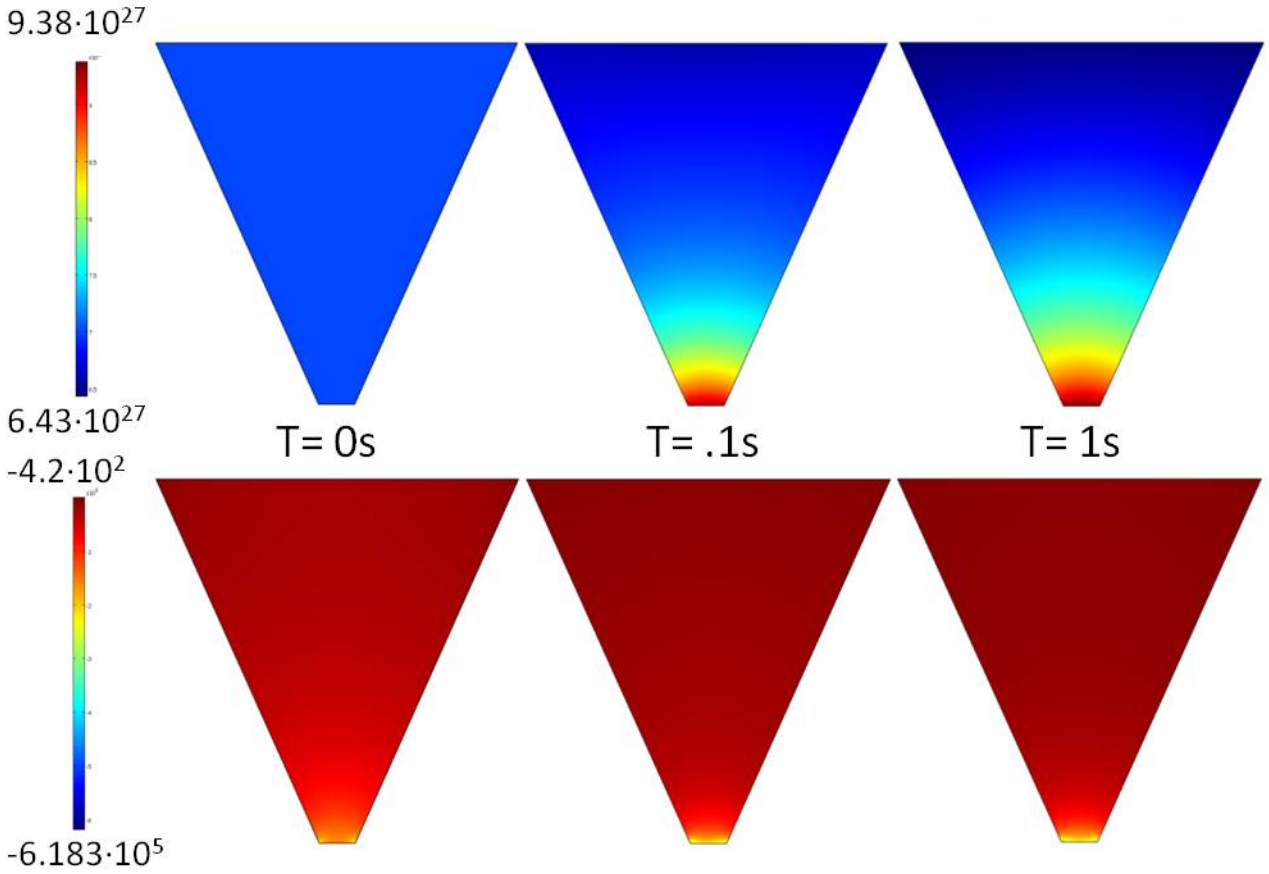

Figure 15: Lithium concentration(top) and electric field(bottom) evolution for the 10x constrictive flow geometry

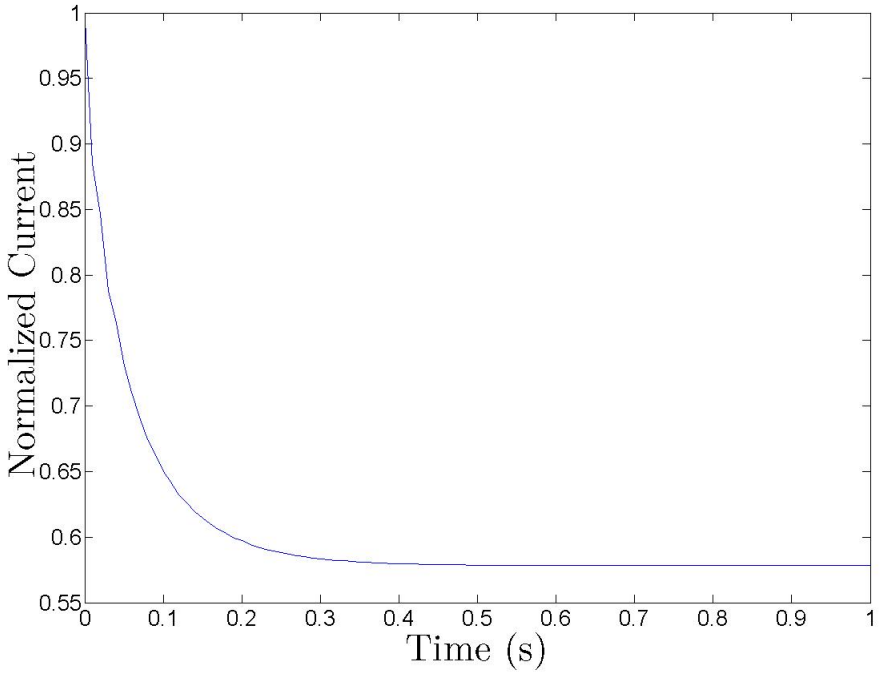

Figure 16: Temporal electronic current response for the 10x constrictive flow geometry

change saturation is due to the amplified diffusivity of lithium as the concentration of lithium approaches stoichiometric levels. Evidence of the diminishing returns with greater ratios in constrictive flow geometries are seen in Figure 17.

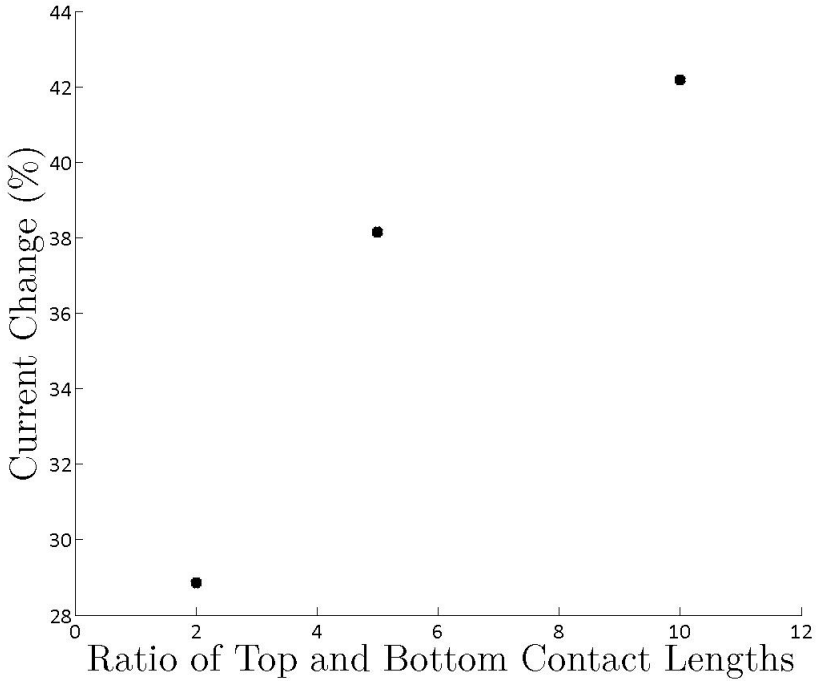

Figure 17: Percent current change for increasing ratios of top and bottom contact lengths. As the ratio is increased, the effect of increased current change begins to diminish as lithium begins to accumulate which results in an increase in ionic diffusion current

A second figure of merit, the speed of the device, is increased with the constrictive flow geometry. Despite having an overall greater change in current, the change in current from .2s to 1s in the constrictive flow geometry memristor is 5.4% while the device in case 1 has a 5.57% current change during the same time period so the constrictive flow geometry memristor has both a greater change in resistance and settles faster. The current change from .2s to 1s in the 5x case is 3.71% as compared to 5.4% in the 2x case, suggesting that more of the current change in the 5x case

occurs before .2s than the 2x case and thus the trend of a faster device with an even greater change in resistance is obtained with the 5x constrictive flow geometry. The speed of the device has once again increased in the case of the 10x constrictive flow geometry. The change in current from .2 to 1 second is 3.18% which is less than that of the 5x case suggesting that the 10x geometry results in a device that rapidly alters resistance These results suggest that constrictive flow geometry memristors not only have a greater change in resistance, but they also facilitate faster resistance modulation.

3.2.4 Case 4: Removal of dopants

As outlined in cases 1-3, limitations in achievable memristance ranges exist any time the total ion (dopant) density in the device cannot be changed. However, this limitation can be overcome if the device is designed with sources and sinks for ions provided these sources and sinks are electrically isolated from the electronic conduction path. By removing ions (dopants), larger resistance ranges can be achieved. The temporal evolution of lithium concentrations of one such device with a constant lithium flux of $2{\cdot}10^{22}$ $\frac{ions}{m^2 s^1}$ extracted from the bottom electrode is shown in Figure 19. The initial lithium concentration is homogeneous throughout the device at $9.99{\cdot}10^{21}$ $\frac{ions}{cm^3}$. At 0.01 seconds, the lithium concentration begins to decrease both at the grounded side of the device where lithium is being extracted and at the positively-biased edge of the device where lithium ions are being drifted away. The depletion of lithium at the edges of the simulated memristor continues at later time steps along with that in the middle portion of the device though this depletion in the middle of the device occurs at a slower rate.

This unique lithium concentration profile gives rise to an involved electric field profile (Figure 20), and demonstrates the complexity involved in a system of mobile dopants in a semiconducting material. On the side of the device where a positive

bias is applied, the electric field has a lower magnitude than that in the rest of the device while the electric field has the highest magnitude at the grounded side of the device. This differing electric field profile in the device for a single given time is due to the interplay of drift and diffusion of holes that result from the gradients in doping created by the movement of lithium ions. Drift and diffusion are competing on the edge of the device where the positive bias is being applied while drift and diffusion coincide on the grounded part of the simulated memristor. Overall, the magnitude of the electric field decreases as the simulation progresses, thus reflecting the decrease in overall resistance in the simulated memristor as shown in Figure 18.

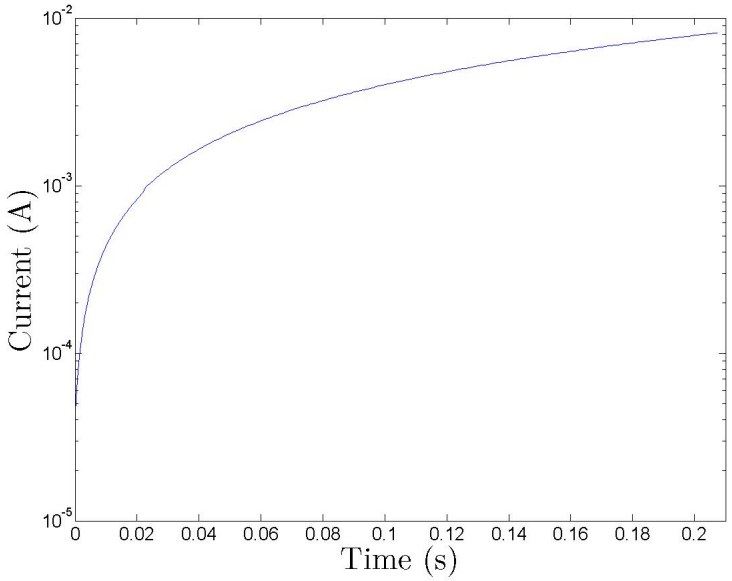

Figure 18: Case 4 current response to a constant bias applied across a simulated $LiNbO_2$ memristor.

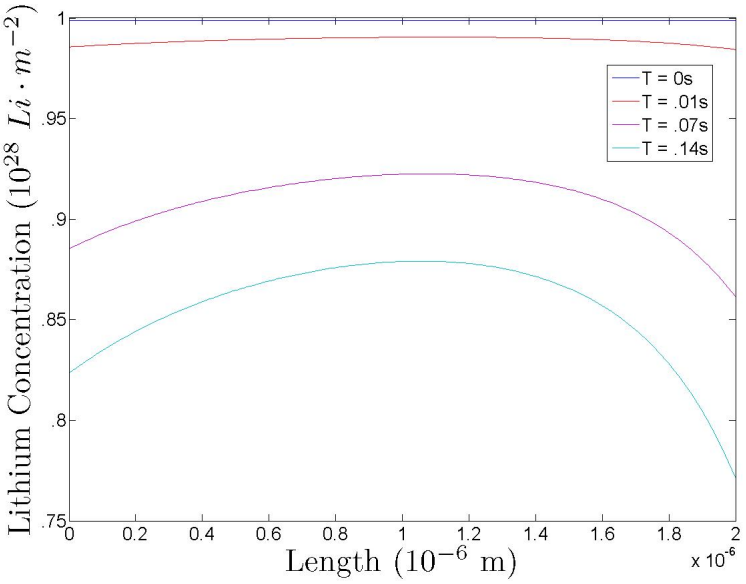

Figure 19: Case 4 temporal and spatial evolution of lithium concentration in an $LiNbO_2$ memristor.

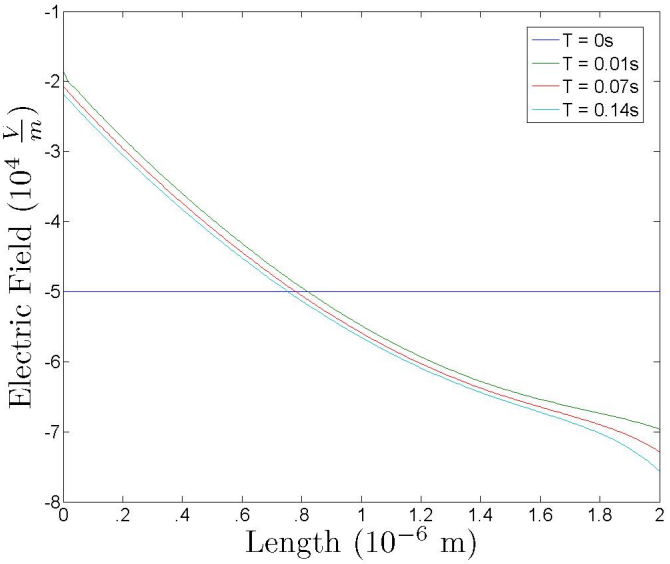

Figure 20: Case 4 temporal and spatial evolution of electric field in an $LiNbO_2$ memristor.

3.2.5 Simulation of a memristor with ring/dot geometry

Once working simulations of simpler geometries was completed, a more realistic simulation was set up to match the geometry of ring/dot memristors as shown in Figure 21.

Seven time steps of the ring/dot geometry memristor simulation are shown in Figure 22. The lithium concentration and electric field profiles are complicated and raise important points about the operation of an analog memristor. At the first time step (T=0 seconds), the lithium concentration in the simulation is uniform at 70% of the maximum packing density of lithium in the $LiNbO_2$ crystal structure. The electric field is at a relatively low level throughout the entire device. The electric field has a peak at the edge of the dot which is due to field crowding forced by the constrictive flow. The initial hole motion is completely drift mediated.

At the next time step, 10 ms, the boundaries at the interface of the metal-semiconductor show a significant change in lithium as shown in Figure 22. This initial change of lithium at the metal-semiconductor interface is important because it describes the mechanism for the operation of smaller (nanometer scale) devices. The lithium content at the semiconductor-metal interface dominates the rapid change in resistance, and the hole motion now includes both components of drift and diffusion. The corresponding electric field corresponding to the 10 ms time step demonstrates a reduction in field at the positively biased central dot associated with the increased doping/Li vacancy concentration.

At later time steps, the lithium concentration continues the trend of rising at the outer electrode-semiconductor interface and falling at the central electrode/semiconductor interface. The lithium concentration in the intermediate region remains relatively constant as the memristor begins to change resistance. The design of this central region distance will thus dictate the time required to "teach a memristor" whereas the absolute change in resistance is dominated by the electrode-semiconductor interface

areas.

As the lithium concentration profile progresses toward a more linear variation, internal built-in electric field profiles dominate the transport. It is interesting to note that there exists two local maxima in electric field at intermediate times (see t=0.09 s). This shows the complexity of even a simple ion motion dominated memristor since around these local maxima, the diffusion component of holes is additive to the drift component in one part of the device and subtractive in another.

As the lithium content increases at the outer electrode edge, a high resistivity region with a dramatically decreased concentration of lithium vacancies (acceptors) is formed. The magnitude of the electric fields in this outer region increases dramatically while there is little field drop across the more conductive inner region. This reduced field in the inner and intermediate region results in a slowing of the Li motion, resulting in the exponential character of the resistance as seen in the case 1 simulation (Figure 4). The field strength in Figure 22, t=0.24 s case is so large the scale had to be changed to 0.3X. This large field/high resistance region near the outer electrode and the initial lithium concentration are both important design criteria for future analog memristors where the change in resistance is to be maximized.

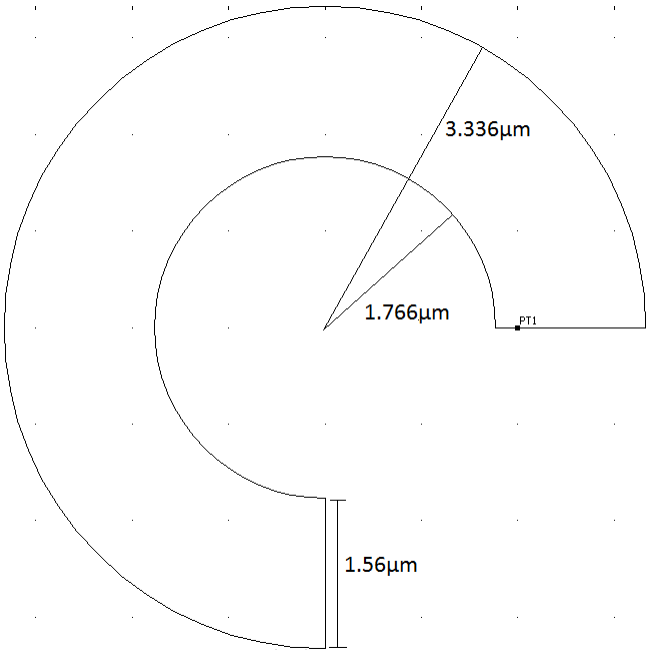

Figure 21: Geometry used in modeling lithium movement in time and space in a ring/dot $LiNbO_2$ memristor.

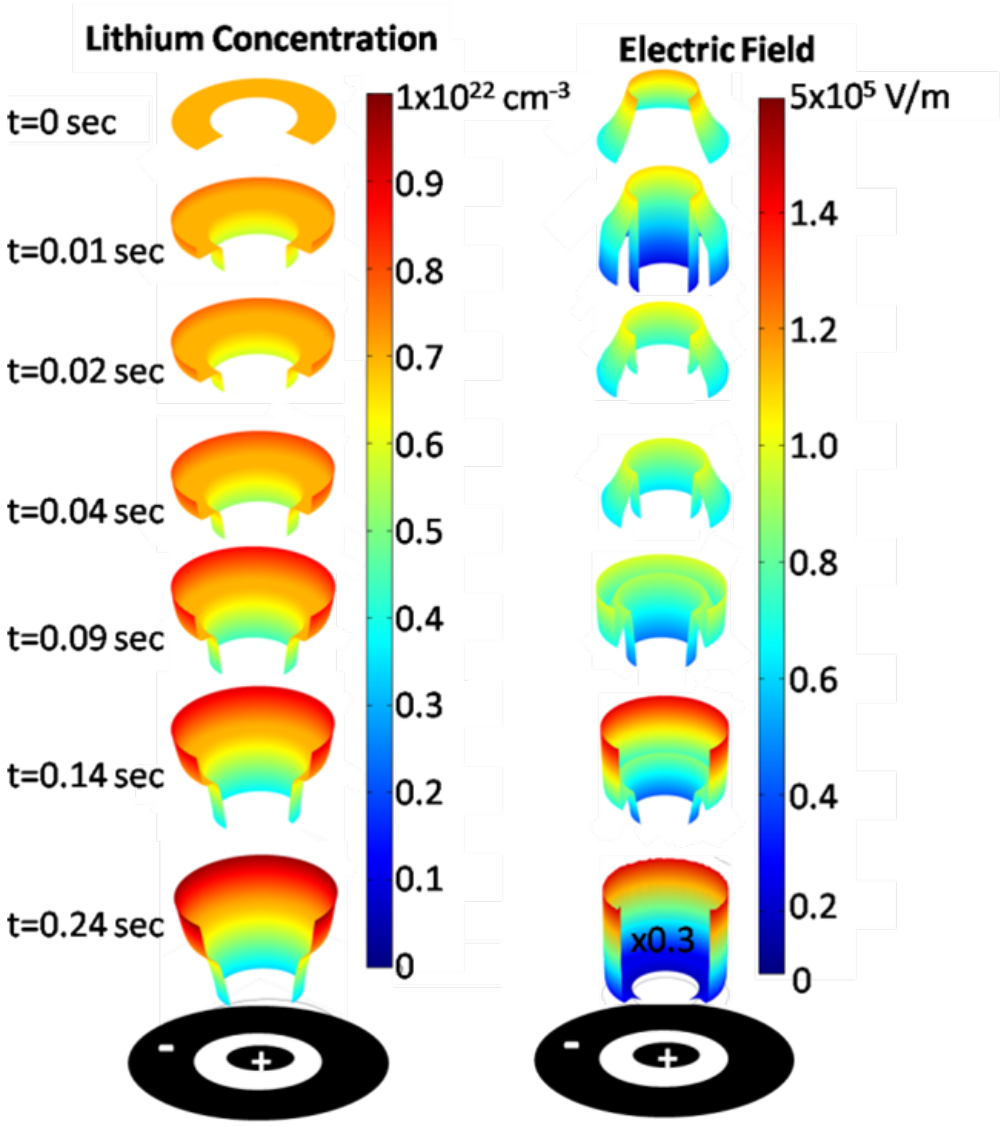

Figure 22: Modeling lithium movement in time and space in an $LiNbO_2$ memristor with a ring/dot geometry. Complicated electric field profiles can arise from a seemingly simple movement of lithium from one side of a memristor to another.

CHAPTER IV

CONCLUSIONS AND FUTURE WORK

4.1 Summary and Contributions

As silicon meets its performance limits, new materials and methods for advancing computing and electronics as a whole are being intensely researched. Memristors are a fusion of these two research areas, with new materials being pursued concurrently to development of novel architectures to take advantage of these new devices.

In order to learn more about the physical mechanisms of analog memristors, a finite element method model has been demonstrated herein that demonstrates the limitations and possible improvements for memristors. Through a greater understanding of these devices, researchers will be able to harness their power and implement them in bio-inspired systems and architectures.

A simple memristor simulation was first demonstrated where the lithium ions (dopants) were confined to the device, but allowed to move in response to a voltage applied across the device. To model a more physical memristor, charge carrier mobility dependence on dopant levels was added to the device, resulting in a simulated device that operated similarly to the first simulation. Thereafter, the effect of varying geometries was modeled, and it was determined that both the speed and the resistance change of the device were improved by increasing the ratio of the top and bottom metal contact lengths in a restrictive flow geometry. Finally, the effect of removing dopants was investigated. It was determined that if the greatest change in resistance is required, then the removal of dopants is the optimal operating regime for an analog memristor.

4.2 Future work

Modeling digital memristors will be the next step in this research. After the digital memristor model is completed, both the digital and analog memristor models will be implemented in a SPICE circuit through the COMSOL-SPICE interface. With this implementation, bio-inspired circuits and computational systems can be simulated to take advantage of using the two devices in tandem.

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